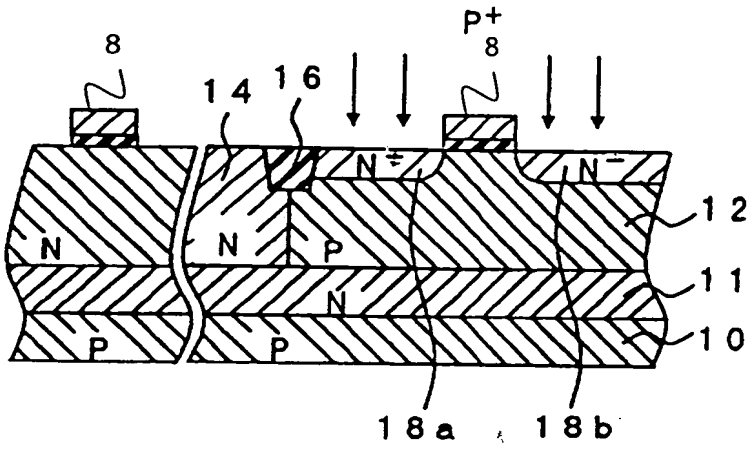


Fig. 17E

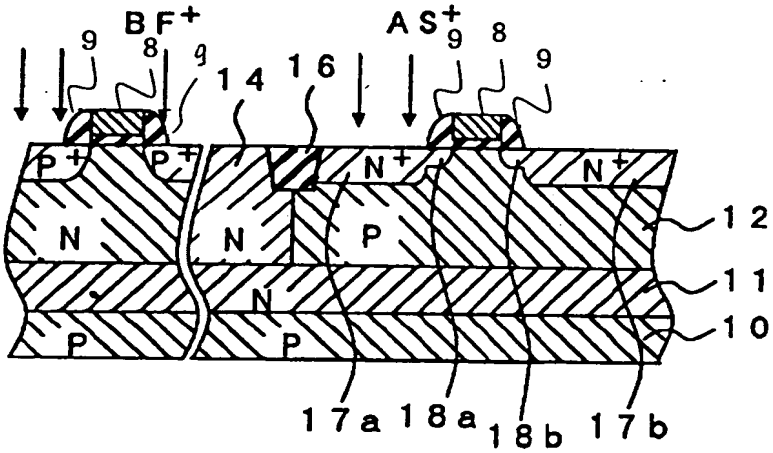


Fig. 17F

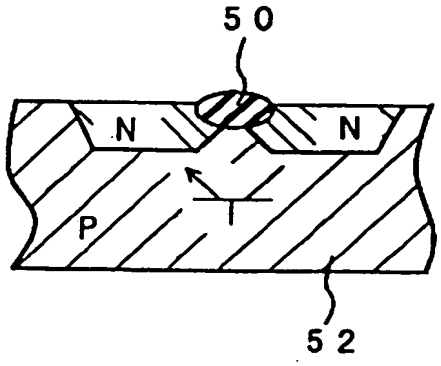


Fig. 1A
PRIOR ART

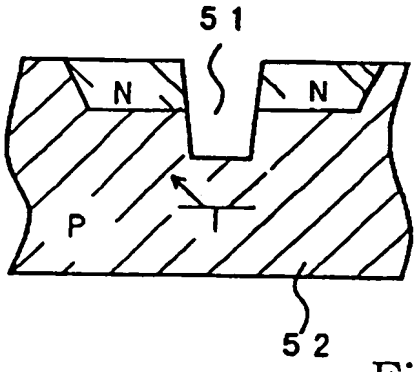


Fig. 1B
PRIOR ART

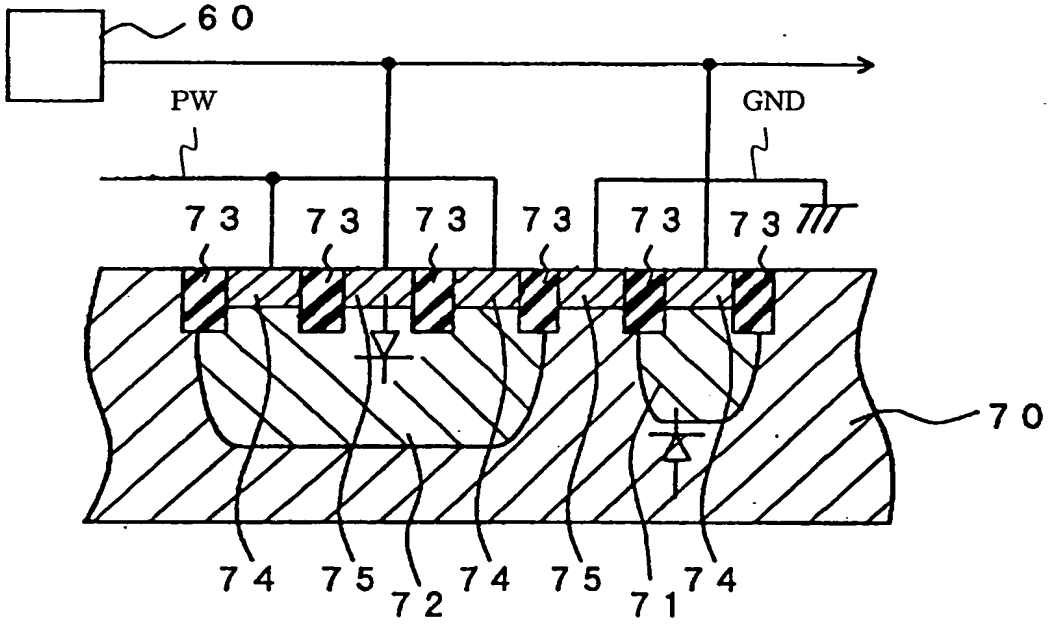


Fig. 2
PRIOR ART

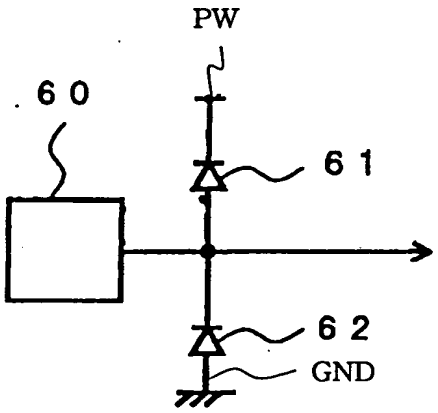


Fig. 3
PRIOR ART

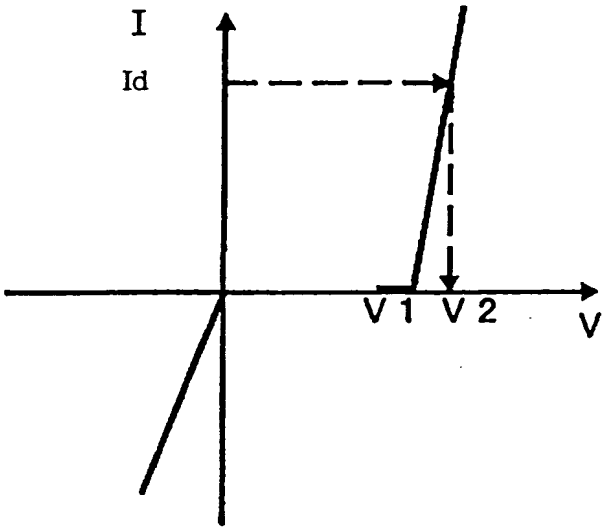


Fig. 4
PRIOR ART

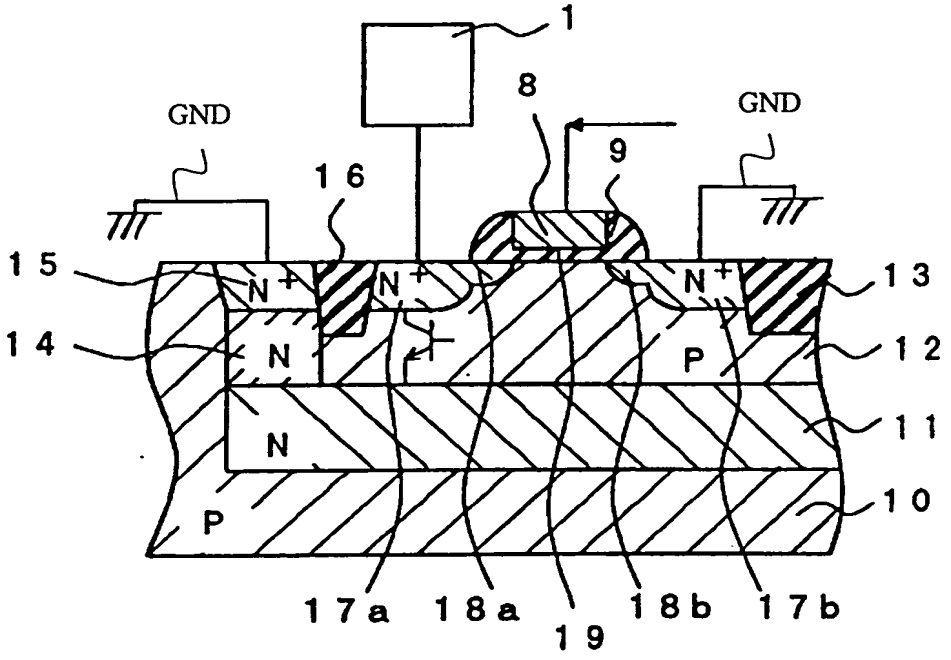


Fig. 5

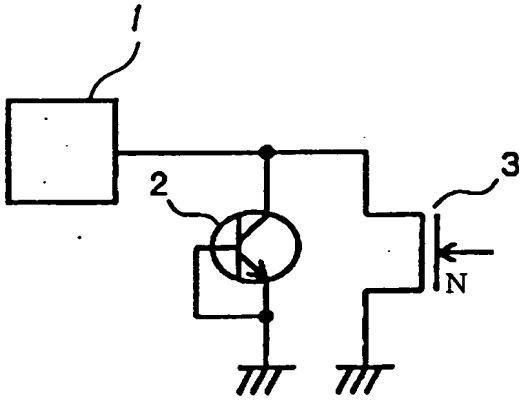


Fig. 6

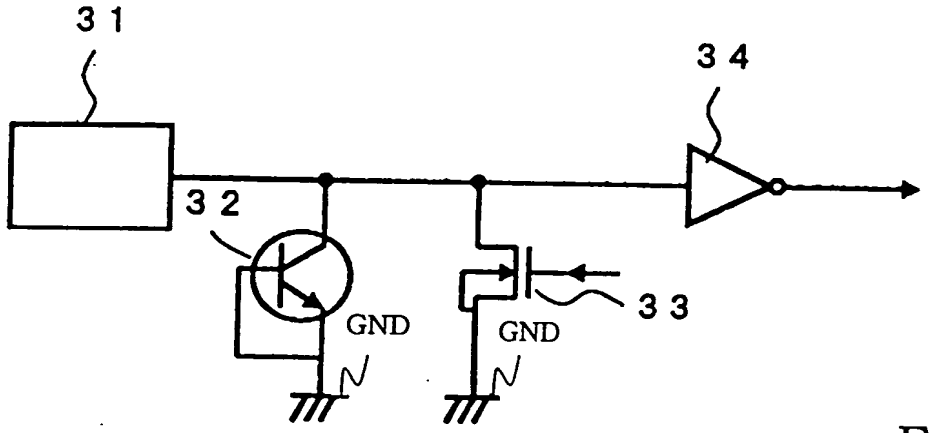


Fig. 15

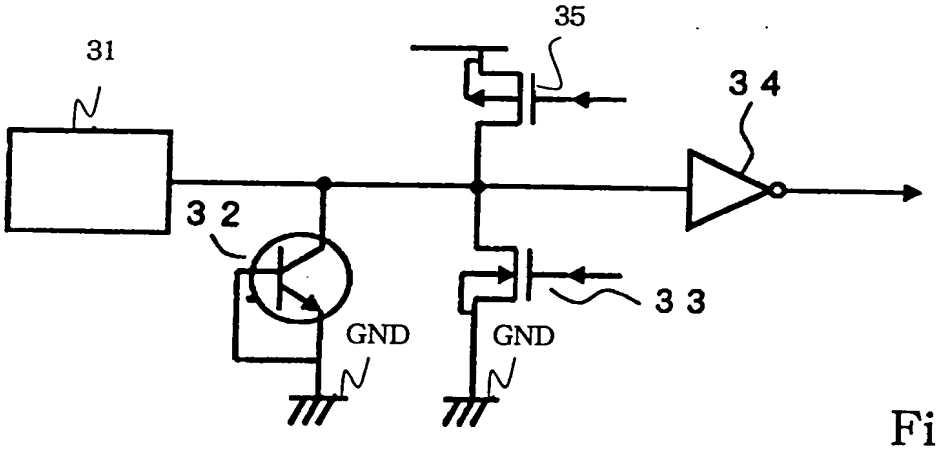


Fig. 16

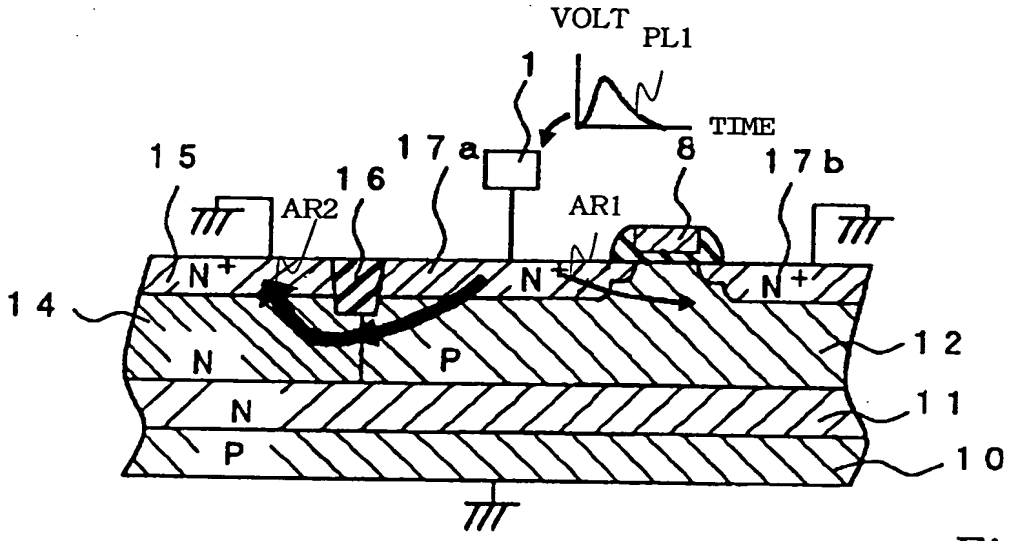


Fig. 7

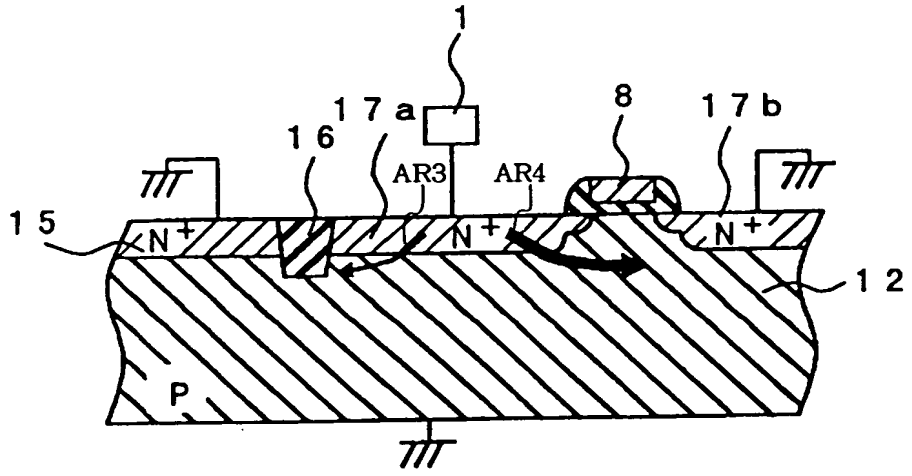


Fig. 8
PRIOR ART

Title: SEMICONDUCTOR DEVICE HAVING PROTECTION CIRCUIT IMPLEMENTED BY BIPOLAR TRANSISTOR FOR DISCHARGING STATIC CHARGE CURRENT AND PROCESS OF FABRICATION
Inventor: Kaoru NARITA
U.S. Appln. No. 09/421,273

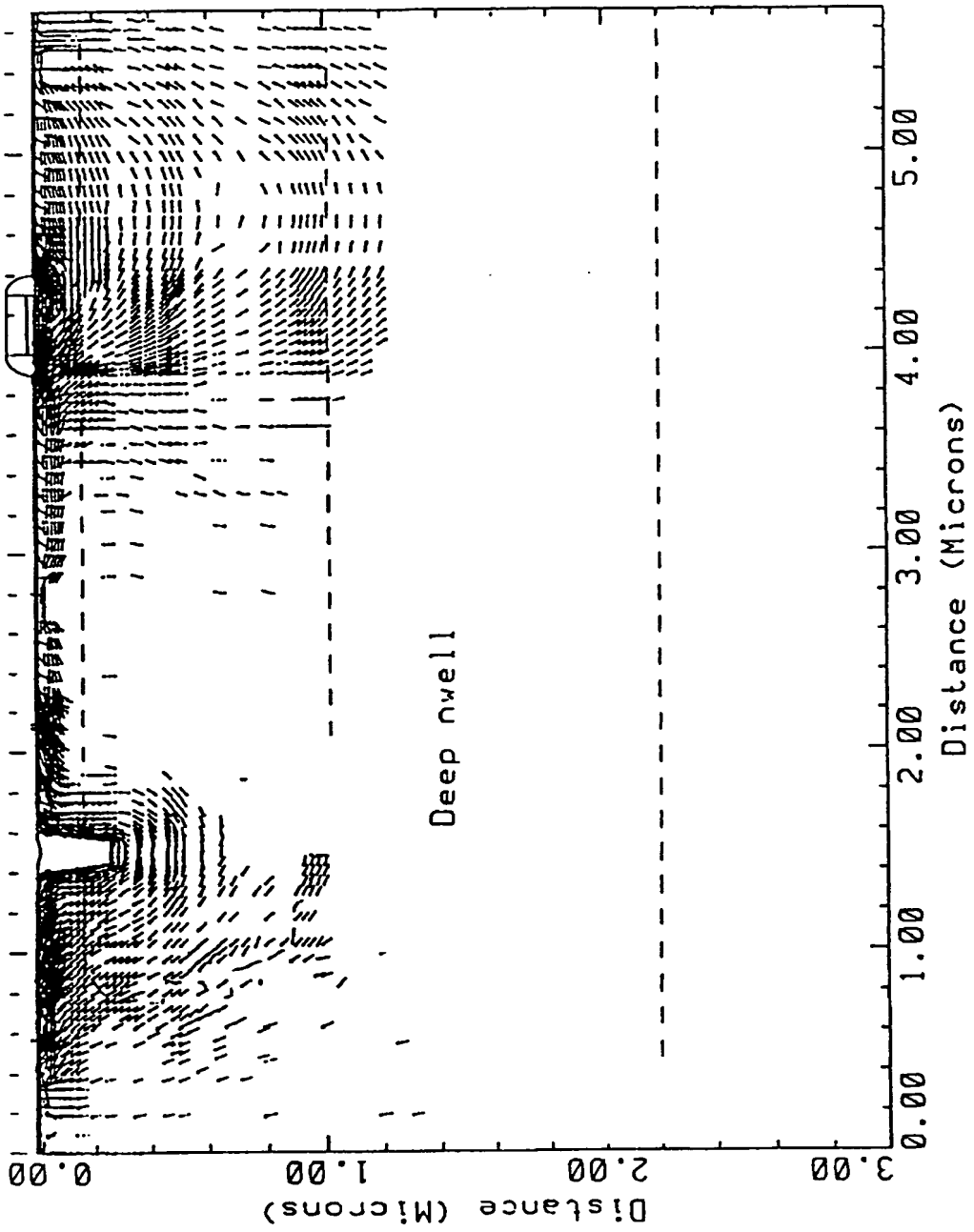


Fig. 9

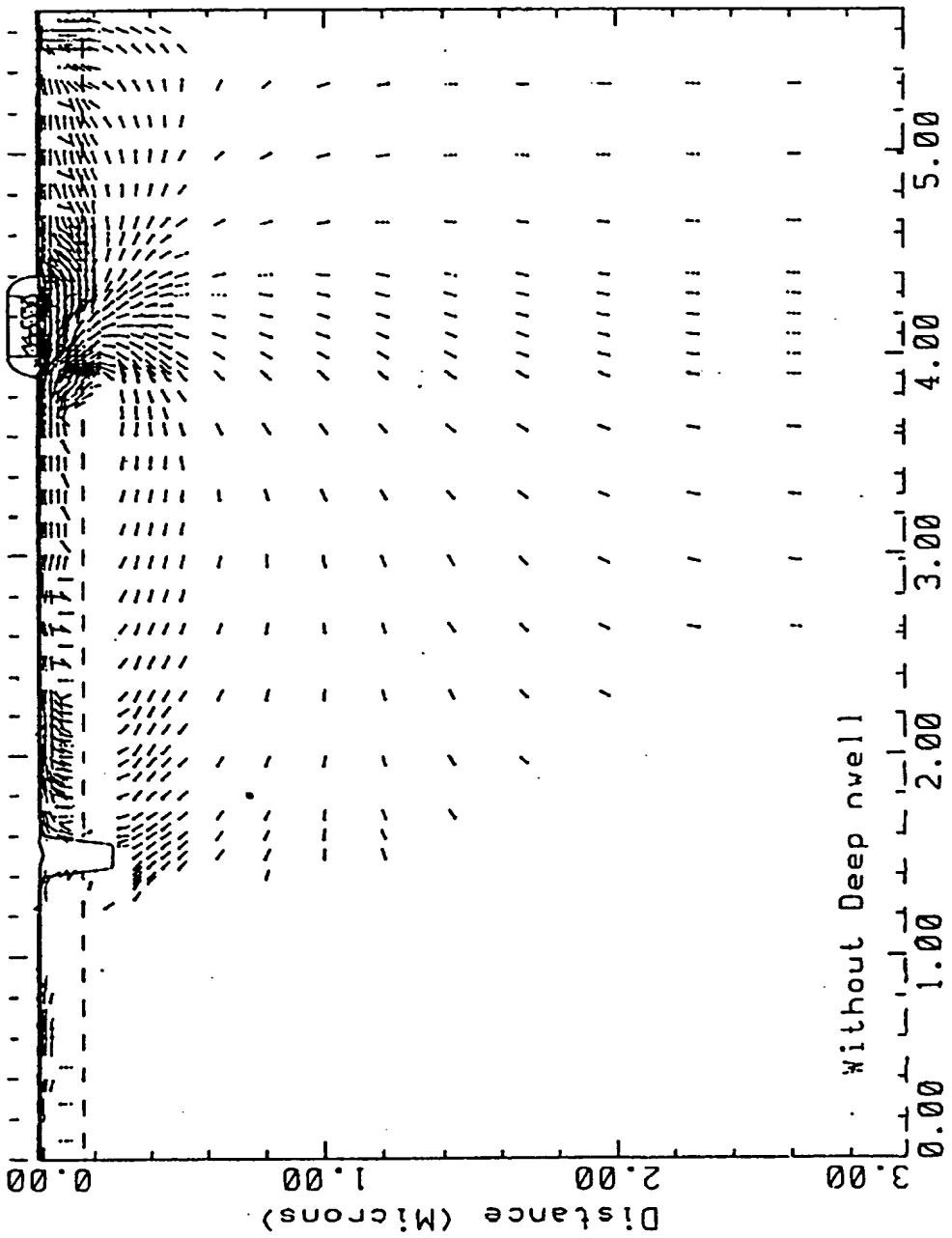
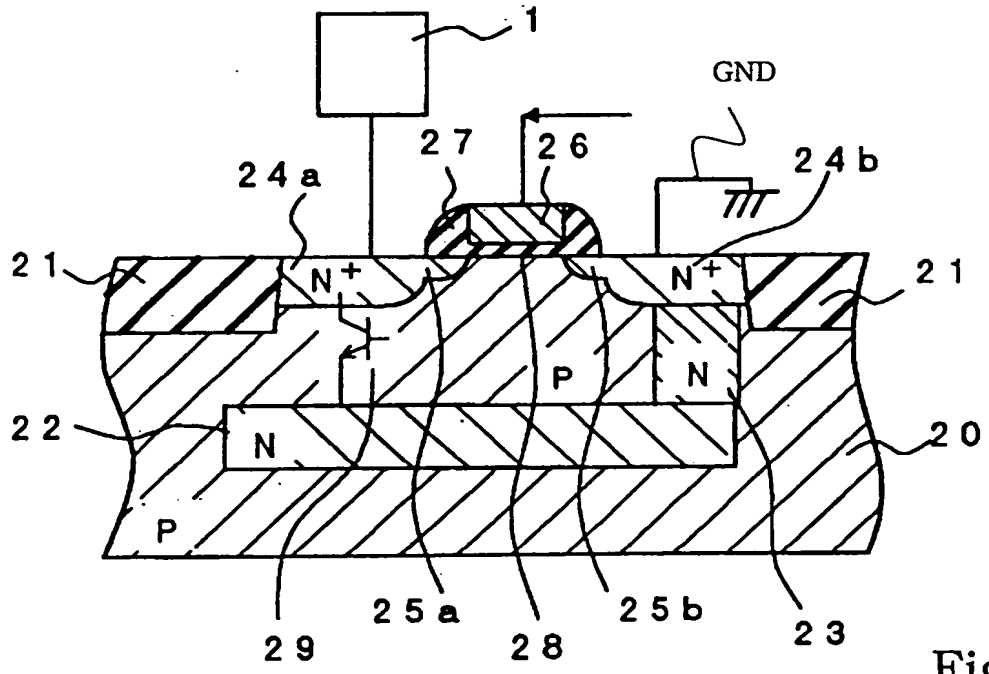


Fig. 10
PRIOR ART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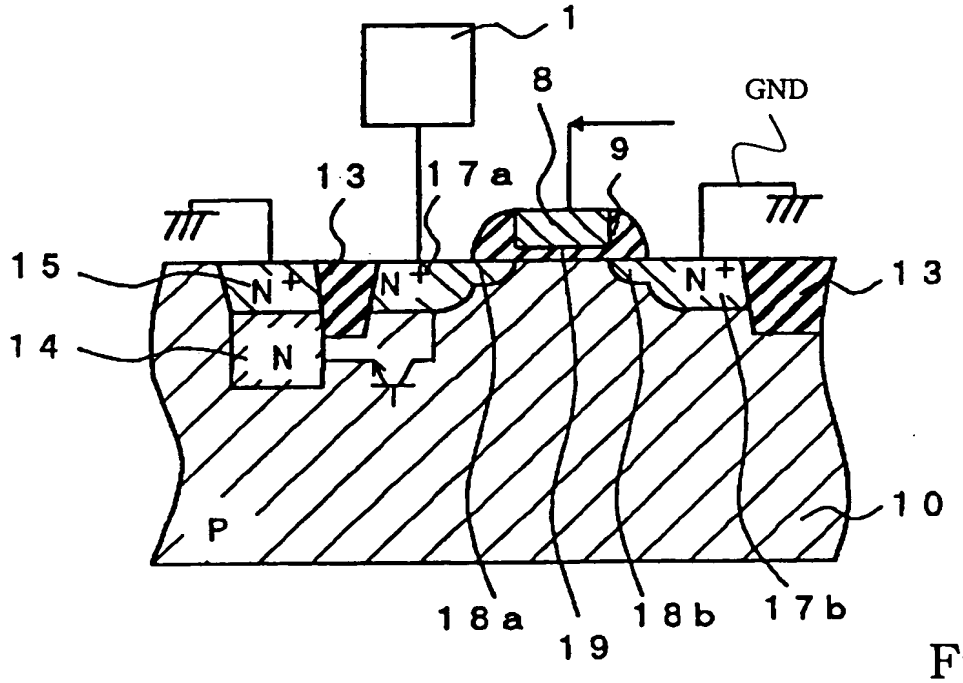
GND
27
26
24a
24b
21
N+
N+
21
P
N
22
N
20
P
29
25a
28
25b
23

Fig. 11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8
GND
9
13
17a
15
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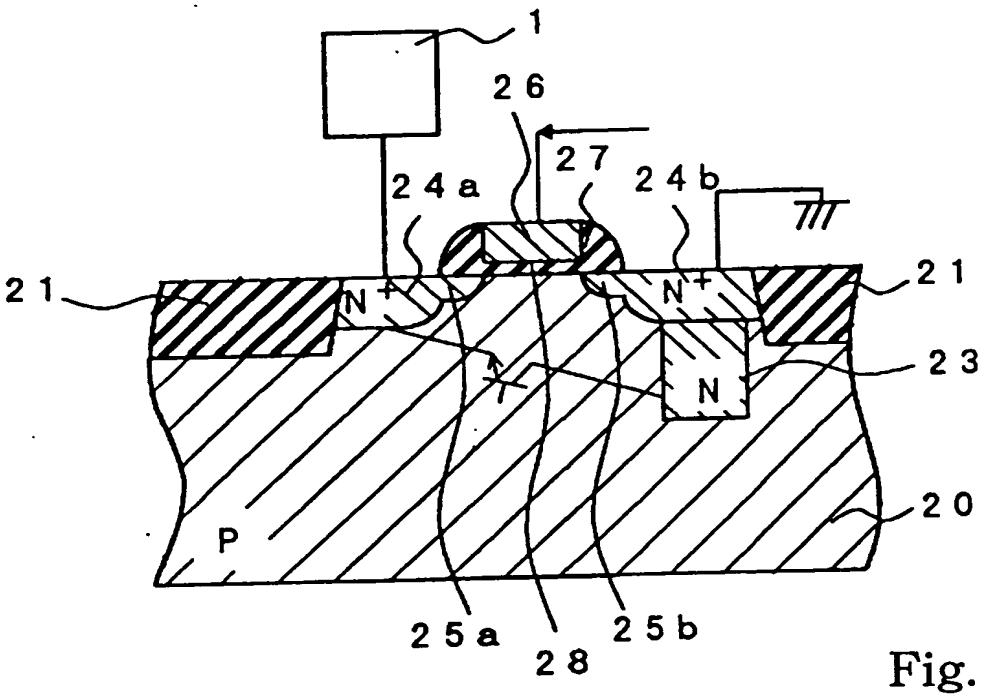
N+
N+
13
14
N
P
10
18a
19
18b
17b

Fig. 12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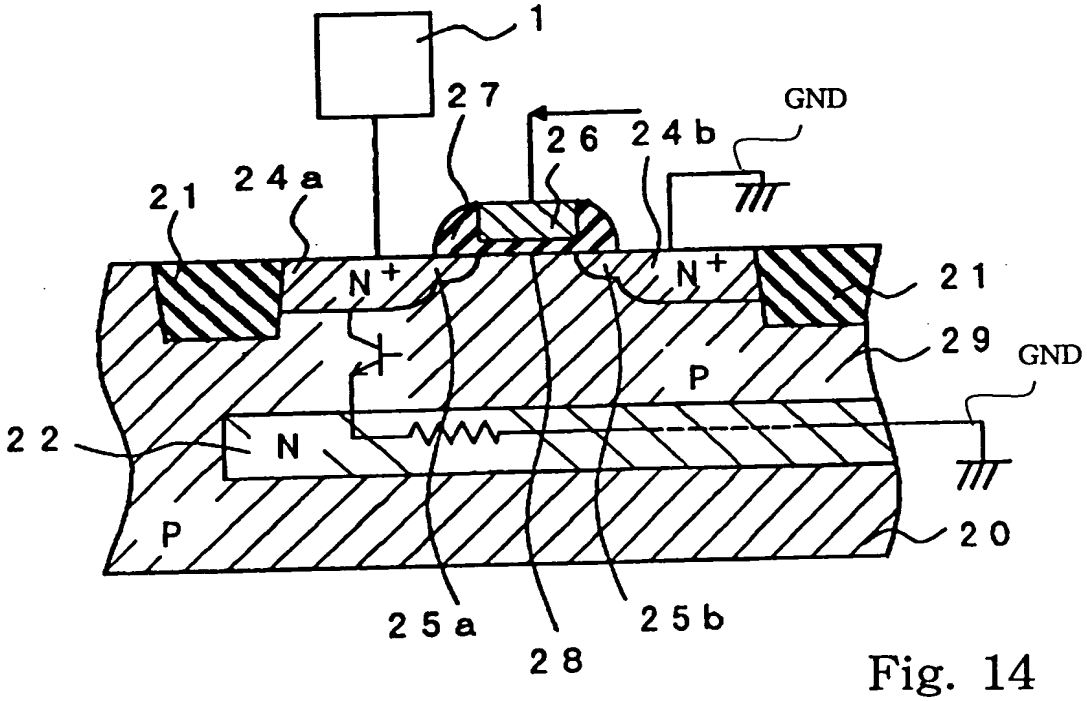
26
27
24a
24b
21
21
N+
N+
23
N
20
P
25a
28
25b

Fig. 13


1
27
GND
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24b
21
24a
N+
N+
21
29
GND
P
22
N
P
20
25a
28
25b

Fig. 14

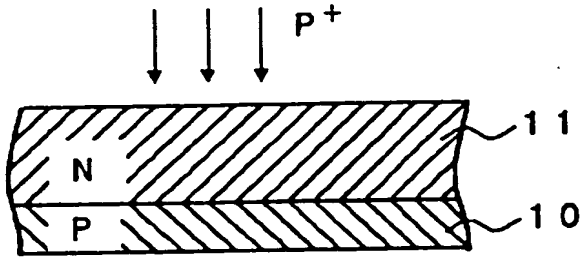

Fig. 17A

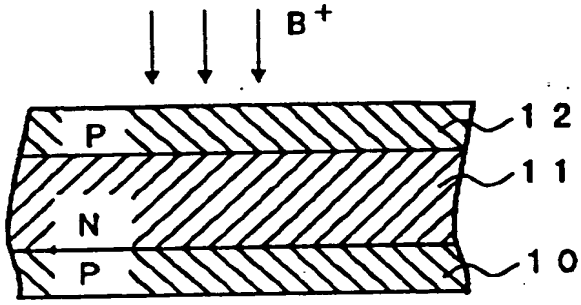

Fig. 17B

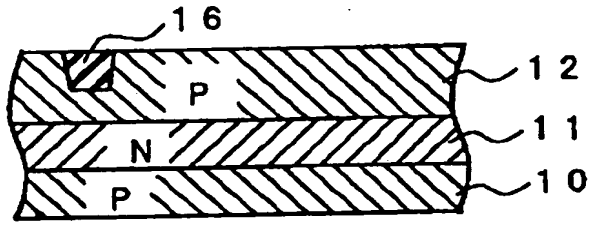

Fig. 17C

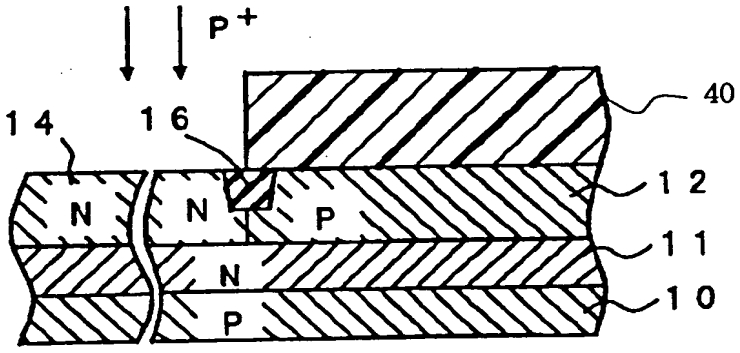

Fig. 17D